#10

7/16/03

Due Date: March 15, 2003

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	
Inventor: Robert J. McMillen et al.	Examiner: Le Hien Luu
Serial #: 09/783,923	Group Art Unit: 2152
Filed: February 14, 2001	Appeal No.: _____
Title: MULTICAST TRANSMISSIONS IN A MULTISTAGE INTERCONNECT NETWORK	

BRIEF OF APPELLANTS

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In accordance with 37 C.F.R. §1.192, Appellants hereby submit the Appellants' Brief on Appeal from the final rejection in the above-identified application, in triplicate, as set forth in the Office Action dated November 25, 2002.

Please charge the amount of $320.00 to cover the required fee for filing this Appeal Brief as set forth under 37 C.F.R. §1.17(c) to Deposit Account No. 50-1673 of NCR Corporation, the assignee of the present application. Also, please charge any additional fees or credit any overpayments to Deposit Account No. 50-1673.

I. REAL PARTY IN INTEREST

The real party in interest is NCR Corporation, the assignee of the present application.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences for the above-referenced patent application.

7/16/03

III. STATUS OF CLAIMS

Claims 154-165 are pending in the application.

Claims 154-165 were rejected under 35 U.S.C. §101 as claiming the same invention as that of claims 86-95 of prior U.S. Patent No. 5,321,813 under the doctrine of statutory double patenting

IV. STATUS OF AMENDMENTS

No amendments have been made subsequent to the final rejection.

V. SUMMARY OF THE INVENTION

Independent claim 154 is directed to a multistage interconnect network comprising: (a) a plurality of switch nodes connected together, each of the switch nodes comprising a first plurality of input ports selectively connectable to a second plurality of output ports, the multistage interconnect network comprising more than $\lceil \log_b N \rceil$ stages of switch nodes, wherein b is a total number of switch node input/output port pairs, N is a total number of network input/output port pairs, and $\lceil \log_b N \rceil$ indicates a ceiling function providing the smallest integer not less than $\log_b$ N, the stages thereby providing a plurality of paths between any network input port and network output port to enhance fault tolerance and lessen contention; (b) the multistage interconnect network including forward channel and back channel signal paths between the switch nodes; (c) the multistage interconnect network capable of multicast transmitting forward channel messages from a source connected to the multistage interconnect network to one or more destinations connected to the multistage interconnect network; (d) the multistage interconnect network capable of combining back channel replies received from the destinations into a single result, wherein the result is transmitted on the back channel to the source.

Independent claim 158 is directed to a method of operating a multistage interconnect network comprising: (a) multicast transmitting forward channel messages from a source connected to the multistage interconnect network to one or more destinations connected to the multistage interconnect network, wherein the multistage interconnect network comprises a plurality of switch nodes connected together, the multistage interconnect network including forward channel and back channel signal paths between the switch nodes, each of the switch nodes comprising a first plurality of input ports selectively connectable to a second plurality of output ports, the

multistage interconnect network comprising more than $\lceil \log_b N \rceil$ stages of switch nodes, wherein b is a total number of switch node input/output port pairs, N is a total number of network input/output port pairs, and $\lceil \log_b N \rceil$ indicates a ceiling function providing the smallest integer not less than $\log_b$ N, the stages thereby providing a plurality of paths between any network input port and network output port to enhance fault tolerance and lessen contention; and (b) combining back channel replies received from the destinations into a single result in the multistage interconnect network, wherein the result is transmitted on the back channel to the source.

Independent claim 162 is directed to a system for transmitting messages, comprising: (a) a plurality of switch nodes connected together in a multistage interconnect network using forward channel and back channel signal paths therebetween; and (b) means for multicast transmitting forward channel messages from a source connected to the multistage interconnect network to one or more destinations connected to the multistage interconnect network; and (c) means for combining back channel replies received from the destinations into a single result, wherein the result is transmitted on the back channel to the source.

With regard to the claims, refer to the specification as follows:

(a) at page 11, line 22 through page 12, line 26 and in FIG. 1 as reference numbers 12, 14, 16 and 20;

(b) at page 14, line 4 through line 14 and in FIG. 1 as reference numbers 12, 32 and 34; and

(c) at page 86, line 12 through page 92, line 143 and in FIG. 25 as reference numbers 12, 14, 16, 18, 30, 32, 34, 36, 56, 74, 96, 98, 108, 110, 114, 120 and 130.

VI. ISSUES PRESENTED FOR REVIEW

1. Whether claims 154-165 are invalid under 35 U.S.C. §101 for claiming the same invention as that of claims 86-95 of prior U.S. Patent No. 5,321,813 under the doctrine of statutory double patenting

VII. GROUPING OF CLAIMS

The rejected claims stand or fall together.

VIII. ARGUMENT

The Examiner rejected claims 154-165 under 35 U.S.C. §101 as claiming the same invention as that of claims 86-95 of prior U.S. Patent No. 5,321,813 under the doctrine of statutory double patenting.

Appellants' attorney respectfully traverses this rejection. Specifically, Appellants' attorney submits that claims 154-165 do not claim the same inventions as claims 86-95 of prior U.S. Patent No. 5,321,813.

In this regard, M.P.E.P §804 states the following:

> In determining whether a statutory basis for a double patenting rejection exists, the question to be asked is: Is the same invention being claimed twice? 35 U.S.C. 101 prevents two patents from issuing on the same invention. "Same invention" means identical subject matter. Miller v. Eagle Mfg. Co., 151 U.S. 186 (1984); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Ockert, 245 F.2d 467, 114 USPQ 330 (CCPA 1957).
>
> A reliable test for double patenting under 35 U.S.C. 101 is whether a claim in the application could be literally infringed without literally infringing a corresponding claim in the patent. In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970). Is there an embodiment of the invention that falls within the scope of one claim, but not the other? If there is such an embodiment, then identical subject matter is not defined by both claims and statutory double patenting would not exist. For example, the invention defined by a claim reciting a compound having a "halogen" substituent is not identical to or substantively the same as a claim reciting the same compound except having a "chlorine" substituent in place of the halogen because "halogen" is broader than "chlorine." On the other hand, claims may be differently worded and still define the same invention. Thus, a claim reciting a widget having a length of "36 inches" defines the same invention as a claim reciting the same widget having a length of "3 feet."

Applying the above analysis to the claims of the present invention, it can be seen that identical subject matter is not being claimed when compared with claims 86-95 of prior U.S. Patent No. 5,321,813.

For the purposes of this comparison, claims 86-95 of prior U.S. Patent No. 5,321,813 are set forth below (and claims 154-165 are reproduced in the appendix):

86. A system for concurrently transferring messages between different ports, comprising:

(a) a plurality of switch nodes, each switch node comprising a first plurality of input ports, a second plurality of output ports, and means for selectively connecting said input ports to said output ports; and

(b) means for connecting the switch nodes together in a multistage interconnect network, the means for connecting comprising forward channel and back channel signal paths; and

(c) multicast means, operative within the network, for transmitting forward channel messages from a source to one or more destinations; and

(d) back channel merge means, within each switch node, for combining back channel replies received from the destinations into a single result, wherein the result is transmitted on the back channel to the source.

87. The system of claim 86, wherein the multicast means comprises means for steering a multicast request for a supercluster to a bounce back point within the network means, wherein all multicast requests to the supercluster use the same bounce back point.

88. The system of claim 87, wherein the means for steering comprises means for steering a multicast request from one supercluster to a destination supercluster through a bounce back point for the destination supercluster.

89. The system of claim 86, wherein the multicast means comprises means for permitting only one multicast message at a time within a supercluster thereby preventing deadlock between competing multicast requests.

90. A method for concurrently transferring messages between different ports of multistage interconnect network, the network comprising a plurality of switch nodes, each switch node comprising a first plurality of input ports, a second plurality of output ports, and means for selectively connecting said input ports to said output ports, the switch nodes connected together via forward channel and back channel signal paths connected to every input and output port, the method comprising the steps of:

(a) transmitting forward channel messages from a source to one or more destinations; and

(b) combining back channel replies received from the destinations into a single result, wherein the result is transmitted on the back channel to the source.

91. The method of claim 90, wherein the transmitting step comprises steering a multicast request for a supercluster to a bounce back point within the network means, wherein all multicast requests to the supercluster use the same bounce back point.

92. The method of claim 91, wherein the steering step comprises steering a multicast request from one supercluster to a destination supercluster through a bounce back point for the destination supercluster.

93. The method of claim 90, wherein the transmitting step comprises permitting only one multicast message at a time within a supercluster, thereby preventing deadlock between competing multicast requests.

94. A system for concurrently transferring messages, comprising:

(a) a multistage interconnect network comprising a plurality of interconnected active logic switch nodes;

(b) each switch node comprising a first plurality of input ports, a second plurality of output ports, and means for selectively connecting said input ports to said output ports;

(c) the multistage interconnect network comprising more than log.sub.b N stages of switch nodes, wherein b is a total number of switch node input/output ports, N is a total number of network input/output ports, and log.sub.b N indicates a ceiling function providing the smallest integer not less than log.sub.b N, the multistage interconnect network providing a plurality of paths between any network input port and network output port to enhance fault tolerance and lessen contention; and

(d) multicast steering means, within each switch node, for routing multicast requests to a specific input port of a specific switch node within the network, so that only one multicast request can occur at a time, thereby preventing deadlock between competing multicast requests.

95. The system of claim 94, further comprising:

(1) means for storing a reply from each network output port in the back channel; and

(2) means for collecting replies from the network output ports and for applying the replies to merge means for synchronously combining all of the replies, wherein the replies are sorted as they propagate through the merge means, so that only the reply having the highest priority is transmitted through the system.

For example, comparing claim 154 of the present application to the independent claims 86, 90 and 94 of prior U.S. Patent No. 5,321,813, it can be seen that the limitations in claims 86, 90 and 94 lack identity with claim 154. Consequently, claims 86, 90 and 94 of the prior U.S. Patent No. 5,321,813 could be literally infringed without literally infringing claim 154 in the present application. Similar arguments can be made for the remaining claims of the present application.

In the final rejection, the Examiner asserts that the combination of claims 94 and 95 of prior U.S. Patent No. 5,321,813 has identical scope of the invention claimed in claim 154 of this

application.

Consider the combination of claims 94 and 95 below:

94. A system for concurrently transferring messages, comprising:
(a) a multistage interconnect network comprising a plurality of interconnected active logic switch nodes;
(b) each switch node comprising a first plurality of input ports, a second plurality of output ports, and means for selectively connecting said input ports to said output ports;
(c) the multistage interconnect network comprising more than log.sub.b N stages of switch nodes, wherein b is a total number of switch node input/output ports, N is a total number of network input/output ports, and log.sub.b N indicates a ceiling function providing the smallest integer not less than log.sub.b N, the multistage interconnect network providing a plurality of paths between any network input port and network output port to enhance fault tolerance and lessen contention; and
(d) multicast steering means, within each switch node, for routing multicast requests to a specific input port of a specific switch node within the network, so that only one multicast request can occur at a time, thereby preventing deadlock between competing multicast requests.

95. The system of claim 94, further comprising:
(1) means for storing a reply from each network output port in the back channel; and
(2) means for collecting replies from the network output ports and for applying the replies to merge means for synchronously combining all of the replies, wherein the replies are sorted as they propagate through the merge means, so that only the reply having the highest priority is transmitted through the system.

Compare the combination of claim 94 and 95 above with claim 154 of this application reproduced below:

154. A multistage interconnect network comprising:
(a) a plurality of switch nodes connected together, each of the switch nodes comprising a first plurality of input ports selectively connectable to a second plurality of output ports, the multistage interconnect network comprising more than $\lceil \log_b N \rceil$ stages of switch nodes, wherein b is a total number of switch node input/output port pairs, N is a total number of network input/output port pairs, and $\lceil \log_b N \rceil$ indicates a ceiling function providing the smallest integer not less than $\log_b$ N, the stages thereby providing a plurality of paths between any network input port and network output port to enhance fault tolerance and lessen contention;

(b) the multistage interconnect network including forward channel and back channel signal paths between the switch nodes;

(c) the multistage interconnect network capable of multicast transmitting forward channel messages from a source connected to the multistage interconnect network to one or more destinations connected to the multistage interconnect network;

(d) the multistage interconnect network capable of combining back channel replies received from the destinations into a single result, wherein the result is transmitted on the back channel to the source.

It can be seen that the limitations in the combination of claims 94 and 95 lack identity with claim 154.

Both claims contain a similar description of the network. However, the combination of claims 94 and 95 also contains the limitations:

multicast steering means, within each switch node, for routing multicast requests to a specific input port of a specific switch node within the network, so that only one multicast request can occur at a time, thereby preventing deadlock between competing multicast requests;

means for storing a reply from each network output port in the back channel; and

means for collecting replies from the network output ports and for applying the replies to merge means for synchronously combining all of the replies, wherein the replies are sorted as they propagate through the merge means, so that only the reply having the highest priority is transmitted through the system.

On the other hand, claim 154 contains the limitations:

the multistage interconnect network including forward channel and back channel signal paths between the switch nodes;

the multistage interconnect network capable of multicast transmitting forward channel messages from a source connected to the multistage interconnect network to one or more destinations connected to the multistage interconnect network;

the multistage interconnect network capable of combining back channel replies received from the destinations into a single result, wherein the result is transmitted on the back channel to the source.

Because of these differences between the limitations in claim 154 and the limitations in the combination of claims 94 and 95, the combination of 94 and 95 of the prior U.S. Patent No.

5,321,813 could be literally infringed without literally infringing claim 154 in the present application.

IX. CONCLUSION

In light of the above arguments, Appellants respectfully submit that the statutory double patenting rejection is erroneous. As a result, a decision by the Board of Patent Appeals and Interferences reversing the Examiner and directing allowance of the pending claims in the subject application is respectfully solicited.

Respectfully submitted,

Robert J. McMillen et al.

By their attorneys,

GATES & COOPER LLP

Howard Hughes Center
6701 Center Drive West, Suite 1050
Los Angeles, California 90045
(310) 641-8797

Date: March 14, 2003

By: _____
Name: George H. Gates
Reg. No.: 33,500

GHG/amb

G&C 30145.1-US-C5

7/16/03

APPENDIX

154. A multistage interconnect network comprising:

(a) a plurality of switch nodes connected together, each of the switch nodes comprising a first plurality of input ports selectively connectable to a second plurality of output ports, the multistage interconnect network comprising more than $\lceil \log_b N \rceil$ stages of switch nodes, wherein b is a total number of switch node input/output port pairs, N is a total number of network input/output port pairs, and $\lceil \log_b N \rceil$ indicates a ceiling function providing the smallest integer not less than $\log_b$ N, the stages thereby providing a plurality of paths between any network input port and network output port to enhance fault tolerance and lessen contention;

(b) the multistage interconnect network including forward channel and back channel signal paths between the switch nodes;

(c) the multistage interconnect network capable of multicast transmitting forward channel messages from a source connected to the multistage interconnect network to one or more destinations connected to the multistage interconnect network;

(d) the multistage interconnect network capable of combining back channel replies received from the destinations into a single result, wherein the result is transmitted on the back channel to the source.

155. The system of claim 154, wherein the multistage interconnect network steers a multicast request for a supercluster to a bounce back point within the network, wherein all multicast requests to the supercluster use the same bounce back point.

156. The system of claim 155, wherein the multistage interconnect network steers a multicast request from one supercluster to a destination supercluster through a bounce back point for the destination supercluster.

157. The system of claim 154, wherein the multistage interconnect network permits only one multicast request at a time within a supercluster, thereby preventing deadlock between competing multicast requests.

158. A method of operating a multistage interconnect network comprising:

(a) multicast transmitting forward channel messages from a source connected to the multistage interconnect network to one or more destinations connected to the multistage interconnect network, wherein the multistage interconnect network comprises a plurality of switch nodes connected together, the multistage interconnect network including forward channel and back channel signal paths between the switch nodes, each of the switch nodes comprising a first plurality of input ports selectively connectable to a second plurality of output ports, the multistage interconnect network comprising more than $\lceil \log_b N \rceil$ stages of switch nodes, wherein b is a total number of switch node input/output port pairs, N is a total number of network input/output port pairs, and $\lceil \log_b N \rceil$ indicates a ceiling function providing the smallest integer not less than $\log_b$ N, the stages thereby providing a plurality of paths between any network input port and network output port to enhance fault tolerance and lessen contention; and

(b) combining back channel replies received from the destinations into a single result in the multistage interconnect network, wherein the result is transmitted on the back channel to the source.

159. The method of claim 158, further comprising steering a multicast request for a supercluster to a bounce back point within the multistage interconnect network, wherein all multicast requests to the supercluster use the same bounce back point.

160. The method of claim 159, further comprising steering a multicast request from one supercluster to a destination supercluster through a bounce back point for the destination supercluster within the multistage interconnect network.

161. The method of claim 159, further comprising permitting only one multicast request at a time within a supercluster, thereby preventing deadlock between competing multicast requests.

162. A system for transmitting messages, comprising:

(a) a plurality of switch nodes connected together in a multistage interconnect network using forward channel and back channel signal paths therebetween; and

(b) means for multicast transmitting forward channel messages from a source connected to the multistage interconnect network to one or more destinations connected to the multistage interconnect network; and

(c) means for combining back channel replies received from the destinations into a single result, wherein the result is transmitted on the back channel to the source.

163. The system of claim 162, further comprising means for steering a multicast request for a supercluster to a bounce back point within the network, wherein all multicast requests to the supercluster use the same bounce back point.

164. The system of claim 163, further comprising means for steering a multicast request from one supercluster to a destination supercluster through a bounce back point for the destination supercluster.

165. The system of claim 163, further comprising means for permitting only one multicast request at a time within a supercluster, thereby preventing deadlock between competing multicast requests.

Gates & Cooper LLP

Howard Hughes Center
6701 Center Drive West, Suite 1050
Los Angeles, California 90045

TO: **Attn: Examiner Le Hien Luu**
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FROM: George H. Gates
OUR REF.: 5104.05

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Applicant:	Robert J. McMillen et al.
Serial No.:	09/783,923
Filed:	February 14, 2001
Group Art Unit:	2141
Our Ref. No.:	5104.05

Per our conversation this morning, please find enclosed the following documents which were FAX-filed in the USPTO on March 14, 2003 in connection with the above referenced case:

- **USPTO Auto Reply – 1pp**
- **G&C facsimile confirmation of transmission - 1pp**
- **Facsimile Cover page to USPTO - 1pp**
- **Transmittal documents – 2pp**
- **Brief of Appellants (one copy only) – 12pp**

By: _____
Name: George H. Gates
Reg. No.: 33,500

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6701 Center Drive West, Suite 1050
Los Angeles, California 90045

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Group Art Unit:	2152
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Howard Hughes Center
6701 Center Drive West, Suite 1050
Los Angeles, California 90045

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Reg. No.: 33,500

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Due Date: March 15, 2003

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Applicant:	Robert J. McMillen et al.	Examiner:	Le Hien Luu
Serial No.:	09/783,923	Group Art Unit:	2152
Filed:	February 14, 2001	Docket:	5104.05
Title:	MULTICAST TRANSMISSIONS IN A MULTISTAGE INTERCONNECT NETWORK		

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GATES & COOPER LLP
Howard Hughes Center
6701 Center Drive West, Suite 1050
Los Angeles, CA 90045
(310) 641-8797

By: _____
Name: George H. Gates
Reg. No.: 33,500
GHG/amb

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